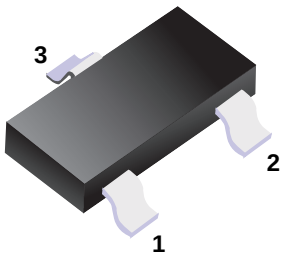
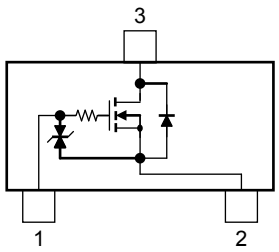
60V N-Channel Enhancement MOSFET

MAIN CHARACTERISTICS

I_D	200mA
V_{DSS}	60V
R_{DSON}-typ(@V_{GS}=10V)	<3.9Ω(Type:2.8mΩ)
R_{DSON}-typ(@V_{GS}=5V)	<8.1mΩ(Type:5.4mΩ)
R_{DSON}-typ(@V_{GS}=4.5V)	<4.7mΩ(Type:3.2mΩ)



1.GATE
2.SOURCE
3.DRAIN



Equivalent Circuit (top view)

SOT23-3L

High Speed Switching Applications

♦ESD protected gate

Marking Code	
2N7002AK	NJ.

Absolute Maximum Ratings Ta = 25℃

Characteristic		Symbol	Rating	Unit
Drain- source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current (Note1)	DC	I_D	200	mA
	Pulse	I_{DP}	760	
Power dissipation(Note 3)		P_D	320	mW
(Note 4)		P_D	1000	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Note 1: The channel temperature should not exceed 150°C during use.

Note 2: Pulse width ≤ 10 μs, Duty ≤ 1%

Note 3: Mounted on an FR4 board
(25.4 mm · 25.4 mm · 1.6 mm, Cu Pad: 0.42 mm^2 x 3)

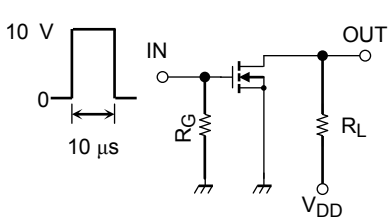
Note 4: Mounted on an FR4 board
(25.4 mm · 25.4 mm · 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics Ta = 25℃

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 250μA ,V_{GS} = 0 V	60	—	—	V
Drain cutoff current		I_{DSS}	V_{Ds} = 60 V, V_{GS} = 0 V	—	—	1	μA
			V_{Ds} = 60 V, V_{GS} = 0 V, Tj=150 °C	—	—	200	
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±2	μA
			V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±0.5	
			V_{GS} = ±5 V, V_{DS} = 0 V	—	—	±0.1	
Gate threshold voltage		V_{th}	I_D = 250 μA V_{DS} = V_{GS}	1.1	—	2.1	V
Forward transfer admittance (Note 5)		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 200 mA	—	450	—	mS
Drain-source ON-resistance (Note 5)		$R_{DS\ (ON)}$	I_D = 100 mA, V_{GS} = 10 V	—	2.8	3.9	Ω
			I_D = 100 mA, V_{GS} = 10 V, Tj=150 °C	—	5.4	8.1	
			I_D = 100 mA, V_{GS}= 5 V	—	3.1	4.4	
			I_D = 100 mA, V_{GS} = 4.5 V	—	3.2	4.7	
Total Gate Charge		$Q_{G(tot)}$	V_{DS} = 30 V, I_D = 200mA V_{GS}= 4.5 V	—	0.27	0.35	nC
Gate-Source Charge		Q_{GS}		—	0.08	—	
Gate-Drain Charge		Q_{GD}		—	0.08	—	
Input capacitance		Ciss	V_{DS} = 10 V, V_{GS}= 0 V, f = 1 MHz	—	11	17	pF
Output capacitance		Coss		—	3	—	
Reverse transfer capacitance		Crss		—	0.7	—	
Switching time	Turn-on delay time	td(on)	V_{DD} = 40 V, I_D= 160 mA V_{GS} = 0 V to 10 V, Rg = 50 Ω	—	2	4	ns
	Rise time	tr		—	3	—	
	Turn-off delay time	$t_{d(off)}$		—	7	14	
	Fall time	t_f		—	24	—	
Drain-source forward voltage (Note 5)		V_{DSF}	I_D = -115 mA, Vgs = 0 V	—	-0.87	-1.2	V

Switching Time Test Circuit

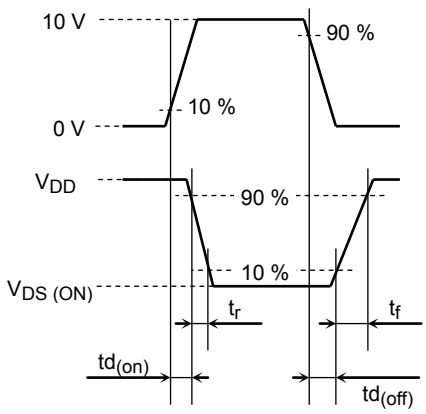
(a) Test Circuit



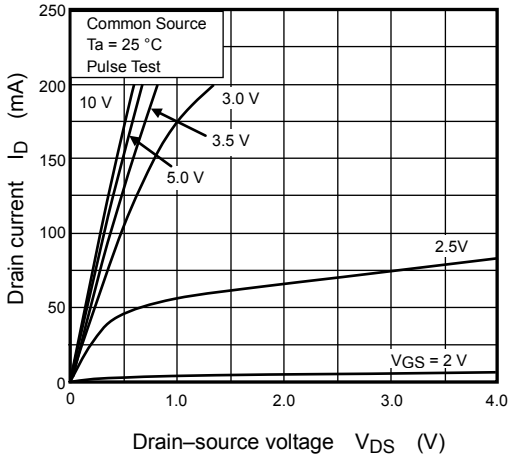
V_{DD} = 40 V
R_G = 50 Ω
D.U. ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

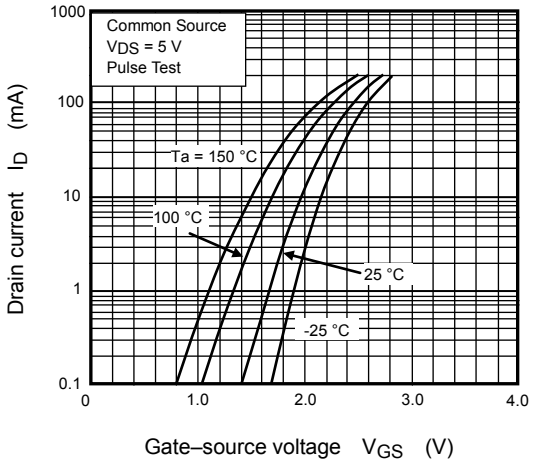
(c) V_{OUT}



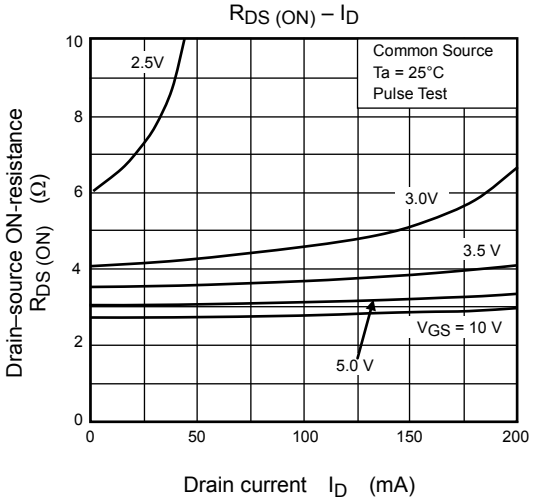
$I_D - V_{DS}$



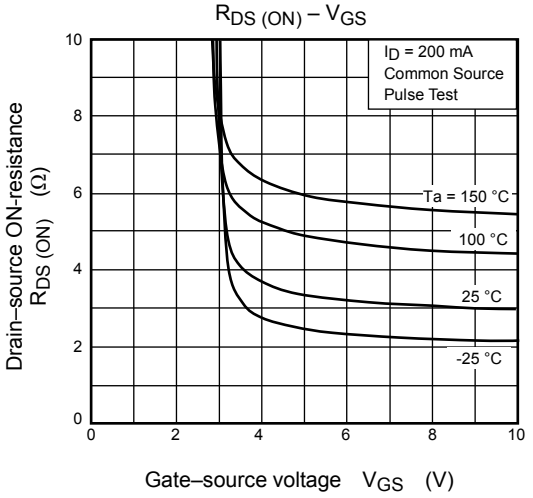
$I_D - V_{GS}$



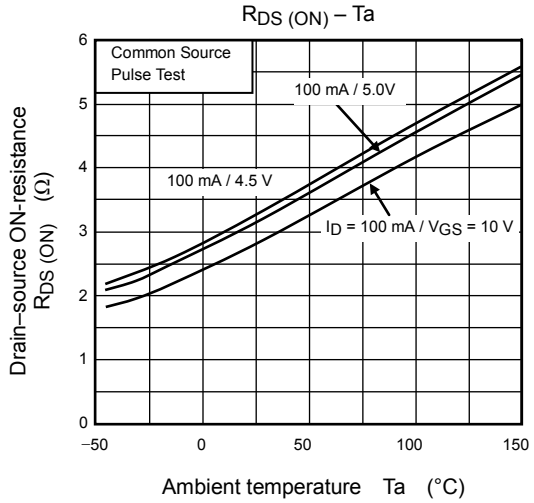
$R_{DS\ (ON)} - I_D$



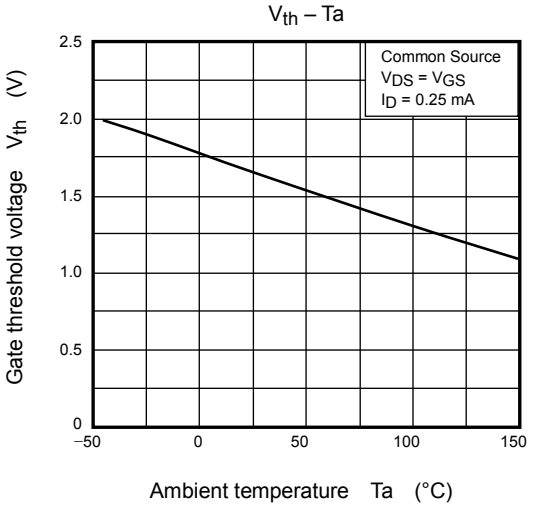
$R_{DS\ (ON)} - V_{GS}$



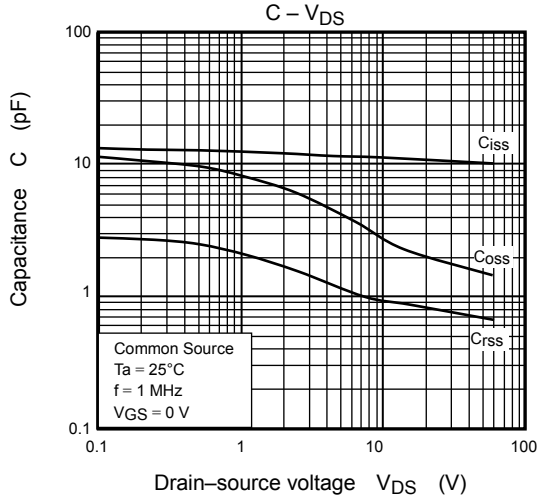
$R_{DS\ (ON)} - Ta$



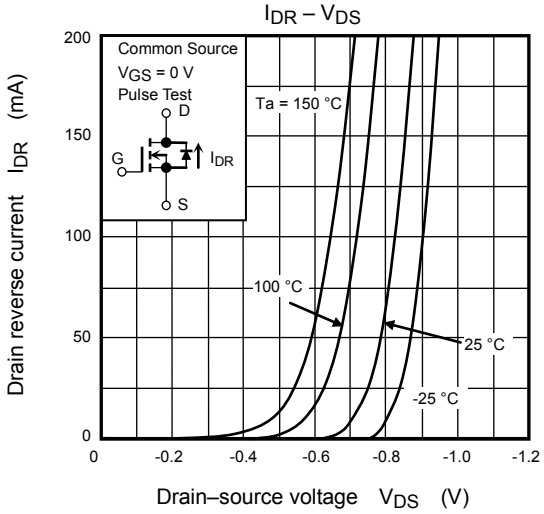
$V_{th} - Ta$



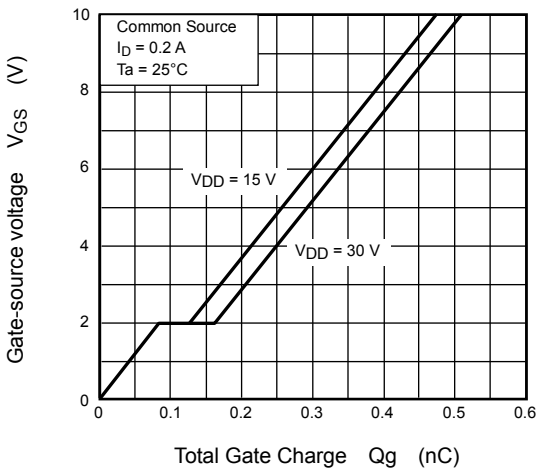
C – V_{DS}



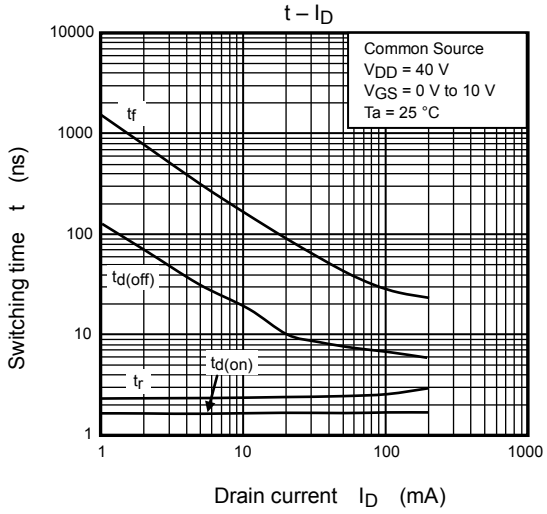
I_{DR} – V_{DS}



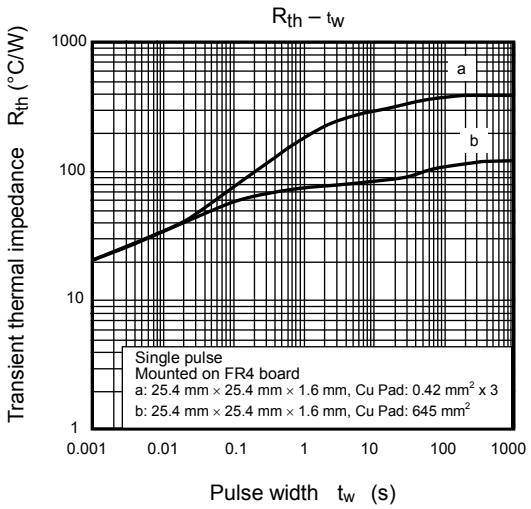
Dynamic Input Characteristic



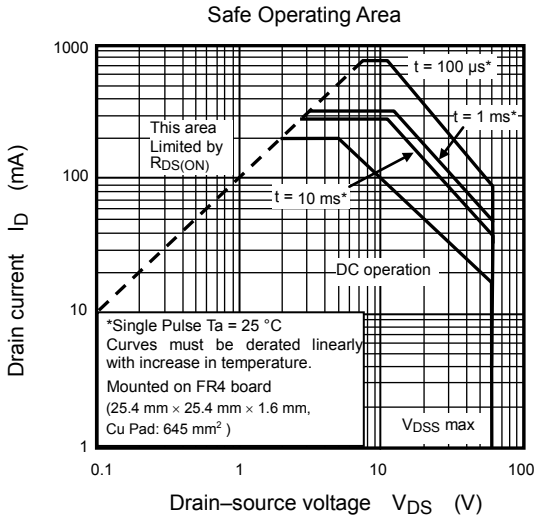
t – I_D



R_{th} – t_w

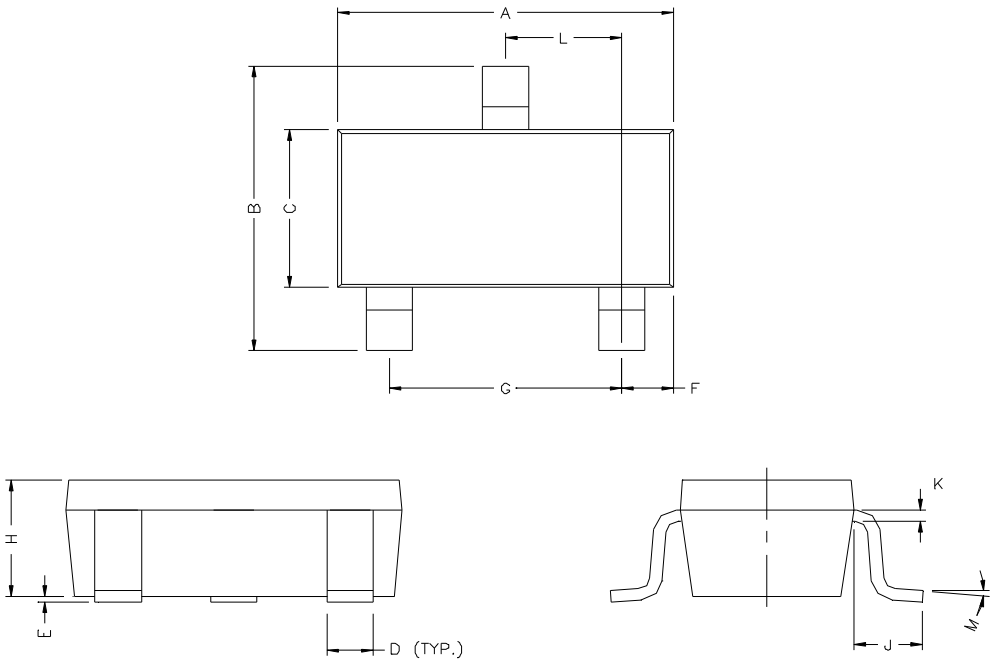


Safe Operating Area



Note: The above characteristics curves are presented for reference only and not guaranteed by production test.

Package Outline SOT23-3L



DIMENSIONS (mm are the original dimensions)

UNIT	A	B	C	D	E	F	G	H	K	J	L	M
mm	2.70 3.10	2.65 2.95	1.50 1.70	0.35 0.50	0 0.10	0.45 0.55	1.9	1.00 1.30	0.10 0.20	0.40 -	0.85 1.15	0° 10°

Summary of Packing Options

Package	Package Description	Packing Quantity	Industry Standard
SOT23-3L	Tape/Reel,7"reel	3000	EIA-481-1